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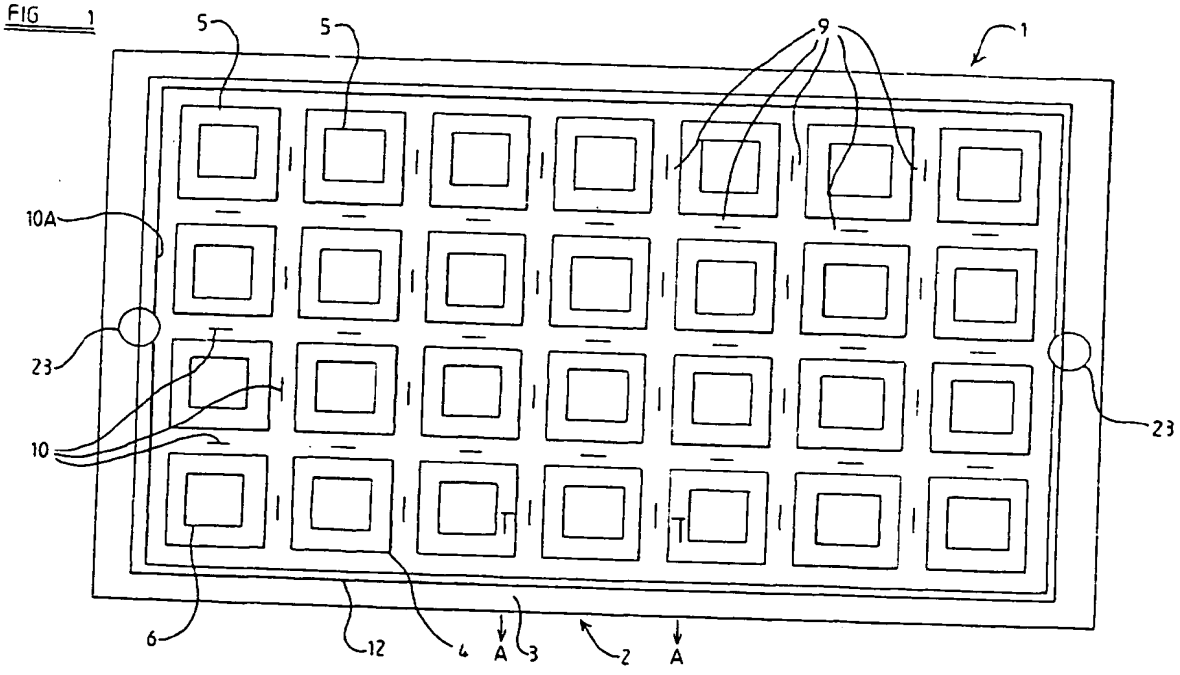
(54) An electronic component package assembly and method of manufacturing the same

(57) An electronic component package assembly comprising: a substantially planar base carrying a number of cavities each defined by a frame; an electronic component attached to the base within each cavity; and a lid fixed to the frame such that, in combination, the base, the lid and each frame define an enclosed volume housing the electronic component.

FIG 1



EP 0 997 934 A2

Description

[0001] THIS INVENTION relates to an electronic component package assembly and method of manufacturing the same. More particularly, the invention relates to a packaging assembly for semiconductor chips and other electrical components including optical electronic components requiring an optical lid.

[0002] Most integrated circuits and discrete semiconductor devices are provided in standard package forms such as DIL (Dual-in-Line) and T018 packages. These types of packages need through holes in a printed circuit board for the their pins or leads to protrude through and to be soldered on the underside of the board to make both electrical and mechanical connection to the board and the tracks on the board.

[0003] Surface mount assembly technology has been developed in which packaged components do not have pins or leads. Instead, the packaged component is placed on a surface of a circuit board, on either side of the board or both sides of the board. Surface mount assembly is regarded as a more refined process than through hole assembly techniques. Finer pitch contacts are possible coupled with the fact that all four sides of a component package are useable thus enabling packages to be smaller with typical space savings in the region of 4:1 when comparing through hole assembly techniques with surface mount assembly techniques.

[0004] Even taking into account the savings in assembly board areas which surface mount assembly techniques provide, the trend has been to increase the density of components which populate a board thereby leaving the component package with higher pin counts which can be up to several hundred pins.

[0005] In the past, some components were used in die or naked form (i.e. unpackaged) in what are called hybrid circuits. Such unpackaged components were usually placed on a ceramics substrate along with necessary tracks, resistors and capacitors. The process for manufacturing the tracks, resistors and some capacitors is known as "print and fire". The "print and fire" technique is especially useful where reproductability of size and weight are critical or power dissipation is high. However, the "print and fire" process is expensive and the requirements of most applications can be met using surface mount assembly technology.

[0006] Pin counts are continuing to rise and are set to increase on average two or three times every five years. One technology which has been developed to help with the high pin count problems is Multi-Chip Modules (MCMs). This technology is also of assistance when dealing with the higher clock speeds now being used in the electronics industry. MCM technology basically packages the high pin count chips that need to interconnect with one another onto a dedicated substrate which can be silicon, alumina or a laminate. The substrate is then put into a package with a more conventional pin pitch for example 1.27mm or 2.54mm to form a chip. The chips used are usually in unpackaged (die/naked) form, although some very small packaged components can also be used within MCMs. The main concept is to have the critical, fast high pin count and high interconnect density circuitry in one or more special MCM assemblies which can then be fitted onto more conventional assemblies.

[0007] MCM technology is still very costly due to the special materials and assembly required. The final size of an MCM is governed by the package size of the overall module which is a function of the number of "out" pins which the module is required to possess and the interconnect density capability required within the MCM. This last factor is dependent on the line spacing capability and chip to substrate connection method within the module.

[0008] The types of interconnection possible between an electronic component and a substrate and/or a package are wire bonding, tape automated bonding and flip-chip which each have their own advantages and disadvantages. In high density assemblies, the power dissipation and the capability to remove heat generated thereby is an important factor.

[0009] With the advent of multi-media computerisation and the Internet as well as a general high growth in optical devices, there is now a need to produce high volume low cost optical packages and interconnects which are capable of being multi-component and used in surface mount technologies and which have automatic handling capability.

[0010] It is an object of this invention to provide a high density surface mount interconnect package for optical devices such as sensors and displays which can be used within MCM at one extreme or as a simple package electronic component at the other extreme.

[0011] It is further object of the invention to provide an electronic component package assembly constructed in arrays.

[0012] It is a further object of the invention to provide an economical electronic components package assembly and method of making the same.

[0013] Another object of the present invention is to reduce the size of electronic component packages compared to the package sizes required for other technologies.

[0014] Accordingly, one aspect of the present invention provides an electronic component package assembly comprising: a substantially planar base carrying a number of cavities each defined by a frame; an electronic component attached to the base within each cavity; and a lid fixed to the frame such that, in combination, the base, the lid and each frame define an enclosed volume housing the electronic component.

[0015] Conveniently, a plurality of tiles are derived from a single panel comprising a base layer attached to a frame layer.

[0016] Conveniently, the lid is manufactured from a transparent material.

[0017] Advantageously, at least one raised portion is

upstanding above each frame to ensure the lid is spaced from the frame by a predetermined gap, the gap being filled with an adhesive to fix the lid to the frame.

[0018] Preferably, the enclosed volume housing the electronic component is at least partly filled with a protective compound.

[0019] Advantageously, the electronic component is a flip-chip, the base being formed with a cut-out substantially adjacent an optical surface of the chip, the cut-out being covered with a transparent material.

[0020] Another aspect of the present invention provides a method of manufacturing a package for an electronic component comprising the steps of: providing a substantially planar base having a number of cavities each defined by a frame; attaching an electronic component to the base within each frame; fixing a lid to the frames such that, in combination, the base, the lid and each frame define an enclosed volume housing the electronic component; and separating from the assembly a number of packages each having a base portion, an electronic component attached to the base, a frame surrounding the electronic component and a lid portion fixed to the frame.

[0021] In order that the present invention may be readily understood, embodiments thereof will now be described, by way of example, with reference to the accompanying drawings in which:

FIGURE 1 is a top view of a tile including package assemblies embodying the present invention;

FIGURE 2 is a side view of the tile of Figure 1;

FIGURE 3 is a detailed cross-section taken along line A-A of Figure 1 showing an electronic component package assembly embodying the present invention forming part of the tile of Figure 1;

FIGURE 4 is a cross-sectional side view of a further electronic component package assembly embodying the present invention and forming part of a tile;

FIGURE 5 is a cross-sectional side view of an electronic component package assembly embodying the present invention in the form of an SO package;

FIGURE 6 is a cross-sectional side view of an electronic component package assembly embodying the present invention in the form of a Ball Grid Array (BGA); and

FIGURE 7 is a schematic representation of an apparatus for manufacturing an electronic component package assembly embodying the present invention.

[0022] Referring to the figures, an electronic component package assembly and method of manufacturing the same will now be described.

[0023] An electronic component package assembly embodying the present invention is produced in the fonn of a panel similar to panels which are used in the manufacture of printed circuit boards. Several hundred packages are accommodated on each panel. The packages are arranged on the panels in the form of several arrays. In one example, each array is a matrix of 4 x 7 packages. Each of these arrays is termed a tile. An example of a tile 1 forming part of a panel (not shown) is shown in Figures 1 and 2.

[0024] A panel comprises a rectangular base substrate 2 of a suitable laminate material such as those commonly used in multi-layer printed circuit boards. The base substrate 2 is metallised on both main surfaces and etched and plated. A second laminate material or frame layer 3 has a single metallised surface. The non-metallised surface of the frame layer 3 is bonded to the base substrate 2. The frame layer 3 is provided with a plurality of substantially square cut-outs 4 in the form of an array. Once the frame layer 3 has been bonded to the base substrate 2, a plurality of tiles 1 are routed out from the panel and after cleaning operations, are ready for subsequent operations such as die attachment and wire bonding. The two layers 2,3 are bonded together in a conventional multi-layer press with post drilling and other operations as required.

[0025] In the example shown in Figure 1, a resultant tile I has an array of cut-outs in a matrix of 4 x 7. Thus, the cut-outs 4 in each tile 1 provide an array of cavities 5 which are capable of receiving an electronic component such as a die therein. As can be seen in Figures 1 and 3, an electronic component 6 is located squarely within each cavity 5 and is seated on the rectangular substrate 2. Preferably, as shown clearly in Figure 3, the electro-component 6 is wire bonded to the etched and plated electrical conducting surface 7 carried on the rectangular substrate 2. In the example shown in Figure 3, the wire bonds 8 connect directly to the etched and plated electrical conducting surface 7. The wire bonds 8 also connect indirectly to other etched conducting surfaces 7A formed on the package through inter-connects in the substrate 2.

[0026] Referring back to Figure 1, the frame layer 3 provides a number of strips 9 which separate adjacent cavities 5. Each such strip 9 is provided with an upstanding lip 10 which runs part way along the strip 9, in parallel therewith. The upstanding lips 10 (or stand-offs) have a predetermined height which is in the order of 0.1mm. A continuous stand-off 10A is also formed around the perimeter of the tile 1. The stand-offs 10,10A are preferably formed on the frame layer 3 prior to bonding to the base substrate 2 by etching and plating, the stand-offs 10,10A thereby being metallised portions.

[0027] The rectangular substrate 2 is conveniently provided with a plurality of vias 11 which serve to interconnect the various conductive layers within the laminate substrate 2. Similar vias 11 may also be formed in

the frame layer 3. As well as providing an inter-connect function, the vias 11 can also be used as thermal vias to conduct heat away from the electrical component 6 to an external pad to which further heat sinks can be attached. If the electronic component 6 does not dissipate too much heat and/or the maximum temperature range of operation thereof is not too high (for example less than 85 degrees C.) then thermal vias may not be necessary.

[0028] The cavity 5 within which each electronic component 6 is mounted is filled or partly filled with a protective compound such as a low viscosity UV-cured acrylic.

[0029] Referring now to Figure 3, each tile 1 is fitted with a glass lid 12. The glass lid 12 sits squarely on the frame layer 3 and is supported thereon by the upstanding lips 10 such that the glass lid 12 is spaced apart from the frame layer 3 by a gap of a predetermined thickness. Conveniently, the glass lid 12 is glued to the frame layer 3, the upstanding lips 10 ensuring that the glass lid 12 is properly spaced apart from the frame layer 3. An example of a particular method of manufacture of the tile I shown in Figures 1 to 3 is described below.

[0030] The glass lid 12 can be modified in a number of ways to produce a selected transmissivity. Thus, the glass lid 12 can be configured as a filter to filter light in pre-selected ranges. The resultant package 13 and method of manufacturing the same are especially suited to the provision of an optoelectronic component as the electronic component 6. The provision of the glass lid 12 is not, however, an essential feature when the package is to be used in non-optical applications.

[0031] The resultant product comprises a tile 1 which carries an array of packages 13. Each package 13 comprises an electronic component 6 packaged within and bounded by a base substrate 2, a plurality of side walls formed by the second substrate material 3 and a lid 12. The electronic component 6 is wire bonded to the package 13 and protectively encased therein. The tiles 1 can then be broken down into individual packages when the various production steps have been completed. Thus, the use of tiles provides a very efficient handling system rather than having to handle small single packages.

[0032] Once the packages 13 have been divided or separated from the tiles 1, they can be embodied into conventional package forms such as surface mount chip carriers, a DIL package 13 having pins or legs 13A as shown in Figure 5 or a ball grid array (BGA) package 13 as shown in Figure 6.

[0033] Referring to Figure 4, the structure of the tile I can be modified to include further laminate materials. In the example shown in Figure 4, a further laminate material 14 is provided on the existing frame layer 3. The further laminate material 14 is formed will cut-outs 15 which are concentric with the cut-outs 4 formed in the frame layer 3. As can be appreciated from Figure 4, the electronic component 6 is wire bonded to an etched conductive surface provided on a step 16 on the frame layer 3. In this embodiment, the upstanding lips 10 are provided on the further laminate material 14. Vias 11 are provided in the respective laminate materials so as to inter-connect the electrically conducting portions thereof.

[0034] In the example shown in Figure 4, the etched conductive layer 7 provided on the base substrate 2 can be made thicker than usual so as to act as a thermal conducting plane to dissipate heat from the electronic component 6. Clearly, the thermal resistance of the conductive layer 7 will depend on the thickness of the layer and the width and lengths of the conducting paths. If further sinking of heat is required, then conductive layer 7 can be clamped or connected to other external heat sinks.

[0035] It should be appreciated that because the packages 13 are provided in the form of an array of packages 13 oil a tile 1, automated handling of the tile 1. is facilitated. It is far easier to handle a tile comprising a fixed array of packages rather than a single package 13. The use of the tile 1 allows accurate alignment during automated stages of production such as the attachment of the electronic component 6 to the tile 1, the wire bonding step, the step of fixing the lid 12 and the step of separating the packages 13 from the tile 1.

[0036] Turning to the particular manufacturing steps for a package 13 and referring to Figure 7, the base substrate 2 is provided and the laminate material 3, complete with cut-outs 4, is glued thereto. The resultant tile 1 provides a plurality of cavities 5 each of which is provided with an electronic component 6. The electronic component is glued to the base substrate 2 (preferably to the etched conductive layer thereon) by one of a number of adhesives commonly used in the semiconductor industry such as, for example, epoxy, polymide and thermoset plastics.

[0037] The electronic component 6 is then wire bonded to a conductive layer or layers within the cavity. Preferably, gold or aluminium wire is used in the wire bonding process using thermosonic or ultrasonic welding techniques. However, it is also possible to use, with modification, tape automated bonding or flip-chip attachments with this invention.

[0038] After wire bonding, the cavity 5 is filled or part filled with a protective compound such as a low viscosity UV-cured acrylic. The protective compound serves to provide structural stability within the package 13.

[0039] Glue is provided along the strips 9 running between adjacent cavities 5 and around the perimeter of the frame layer 3. The glue covers the strips 9 and the perimeter and provides a bead of glue which is slightly greater in thickness than the height of the upstanding lips 10.

[0040] In this condition, the assembled tile 1 is located on the base of a sealing jig 20 which is connected to a vacuum 21. The base of the sealing jig 20 has two locating pins 22 upstanding therefrom. The two pins 22 are of slightly different sizes. Each end of the assembled

tile 1 is provided with a locating hole 23 (see Figure 1). Preferably, the holes 23 are of slightly different sizes such that the tile 1 can only be inserted in one orientation on the base of sealing jig 20. The tile 1 is inserted on the base of the sealing jig 20 with the two locating pins 22 from the base passing through the locating holes 23 in the tile 1.

[0041] The glass lid 12 is presented to the top of the sealing jig 20 and is held thereto by vacuum pressure provided by the vacuum 21. The top of the jig 20 is presented to the base of the jig 20 such that the glass lid 12 is immediately above and registered with the frame layer 3. The glass lid 12 is dropped onto the tile 1 below. The upstanding lips 10 ensure that the glass lid 12 is spaced apart from the frame layer 3 by the desired distance to ensure that the glue properly adheres the glass lid 12 to the frame layer 3. Once the glue has wetted to the glass lid, a small back pressure is applied by the top jig to push the glass lid onto the upstanding lips 10. The upstanding lips 10 ensure that the correct thickness of glue is maintained uniformly across the tile 1. Whilst still in the jig 20, the glass is secured by curing the glue, preferably a low viscosity UV-cured acrylic, by exposure to ultraviolet light. The vacuum is then released and the tile 1 is removed for the final stage of package separation.

[0042] In the package separation stage, the individual packages 13 are cut from the tile 1 by cutting along the centres of the strips 9 separating adjacent cavities 5 - i. e. along the lines defined by the upstanding lips 10. The vias 11 are also located such that their centres fall along the cut line thus forming castellations down to the bottom metal layer 7A on which the package footprint has been formed. The castellations are used for solder paste soldering connections. The cut-outs 4 in the frame layer provide a frame around each of the electronic components.

[0043] It is also envisaged that further wire bonding sites can be provided within each cavity 5 by providing multiple steps in the cavity walls, i.e. on the sides of the package frame in a similar manner to the step 16 shown in Figure 4.

[0044] Whilst specific embodiments of packages are shown in Figures 5 and 6, it will be apparent to those in the industry and skilled in the art of PCB manufacture, that numerous versions are possible whilst adhering to the basic principles of the invention.

[0045] It is envisaged that, in an alternative embodiment, the cavities 5 can be milled out from a single laminate material although this is not preferred.

[0046] In a flip-chip embodiment of the present invention, the face of the flip-chip 6 is attached to the base 2, both mechanically and electrically, by means of a plurality of micro-balls located around the periphery of the face of the chip 6. In the case of the chip 6 being an electro-optical chip, the base 2 is formed with a cut-out. The cut-out is located substantially adjacent an optical surface of the chip and is covered with a glass lid or insert. In this embodiment, the lid 12 need not be made from a transparent material and is preferably pre-bonded to the frame layer 3 prior to attachment to the base 2, the flip-chip having already been attached to the base 2.

[0047] In the present specification "comprise" means "includes or consists of" and "comprising" means "including or consisting of".

[0048] The features disclosed in the foregoing description, or the following claims, or the accompanying drawings, expressed in their specific forms or in terms of a means for performing the disclosed function, or a method or process for attaining the disclosed result, as appropriate, may, separately, or in any combination of such features, be utilised for realising the invention in diverse forms thereof.

Claims

1. An electronic component package assembly comprising: a substantially planar base carrying a number of cavities each defined by a frame; an electronic component attached to the base within each cavity; and a lid fixed to the frame such that, in combination, the base, the lid and each frame define an enclosed volume housing the electronic component.

2. A package assembly according to the previous claim, wherein the frames are provided on a frame layer attached to the base.

3. A package assembly according to Claim 1 or 2, wherein a plurality of frames are provided which are arranged in an array on the base.

4. A package assembly according to Claim 3, wherein a plurality of tiles are derived from a single panel comprising a base layer attached to a frame layer.

5. A package assembly according to any preceding claim, wherein the base comprises one or more layers of a laminate material.

6. A package assembly according to any preceding claim, wherein the frames comprise one or more layers of a laminate material.

7. A package assembly according to any preceding claim, wherein each frame is of a substantially rectangular configuration.

8. A package assembly according to any preceding claim, wherein the lid is manufactured from a transparent material.

9. A package assembly according to any preceding

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claim, wherein the lid is manufactured from glass.

10. A package assembly according to Claim 8 or 9, wherein the transparent material has a selected transmissivity.

11. A package assembly according to any one of Claims 8 to 10, wherein the electronic component is an optical device.

12. A package assembly according to any preceding claim, wherein at least one raised portion is upstanding above each frame to ensure the lid is spaced from the frame by a predetermined gap, the gap being filled with an adhesive to fix the lid to the frame.

13. A package assembly according to any preceding claim, wherein the enclosed volume housing the electronic component is at least partly filled with a protective compound.

14. A package assembly according to Claim 13, wherein the protective compound is as a low viscosity UV-cured acrylic.

15. A package assembly according to any preceding claim, wherein the base has at least one etched electrically conducting surface and the electronic component is electrically connected thereto.

16. A package assembly according to any preceding claim, wherein the frame has at least one etched surface.

17. A package assembly according to any preceding claim, wherein one or more vias are provided through the base to interconnect any conducting layers therein or thereon.

18. A package assembly according to any preceding claim, wherein vias are provided through the frame to interconnect any conducting layers therein.

19. A package assembly according to any preceding claim, wherein thermal vias are provided through the base to dissipate heat from the electronic component.

20. A package according to any preceding claim, wherein the electronic component is a flip-chip, the base being formed with a cut-out substantially adjacent an optical surface of the chip, the cut-out being covered with a transparent material.

21. A electronic component package having a base portion, an electronic component attached to the base, a frame surrounding the electronic component and a lid portion fixed to the frame, which package comprises a part of a package assembly according to any preceding claim.

22. A method of manufacturing a package for an electronic component comprising the steps of: providing a substantially planar base having a number of cavities each defined by a frame; attaching an electronic component to the base within each frame; fixing a lid to the frames such that, in combination, the base, the lid and each frame define an enclosed volume housing the electronic component; and separating from the assembly a number of packages each having a base portion, an electronic component attached to the base, a frame surrounding the electronic component and a lid portion fixed to the frame.

23. An electronic component package assembly substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

24. A method of manufacturing a package for an electronic component package assembly substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

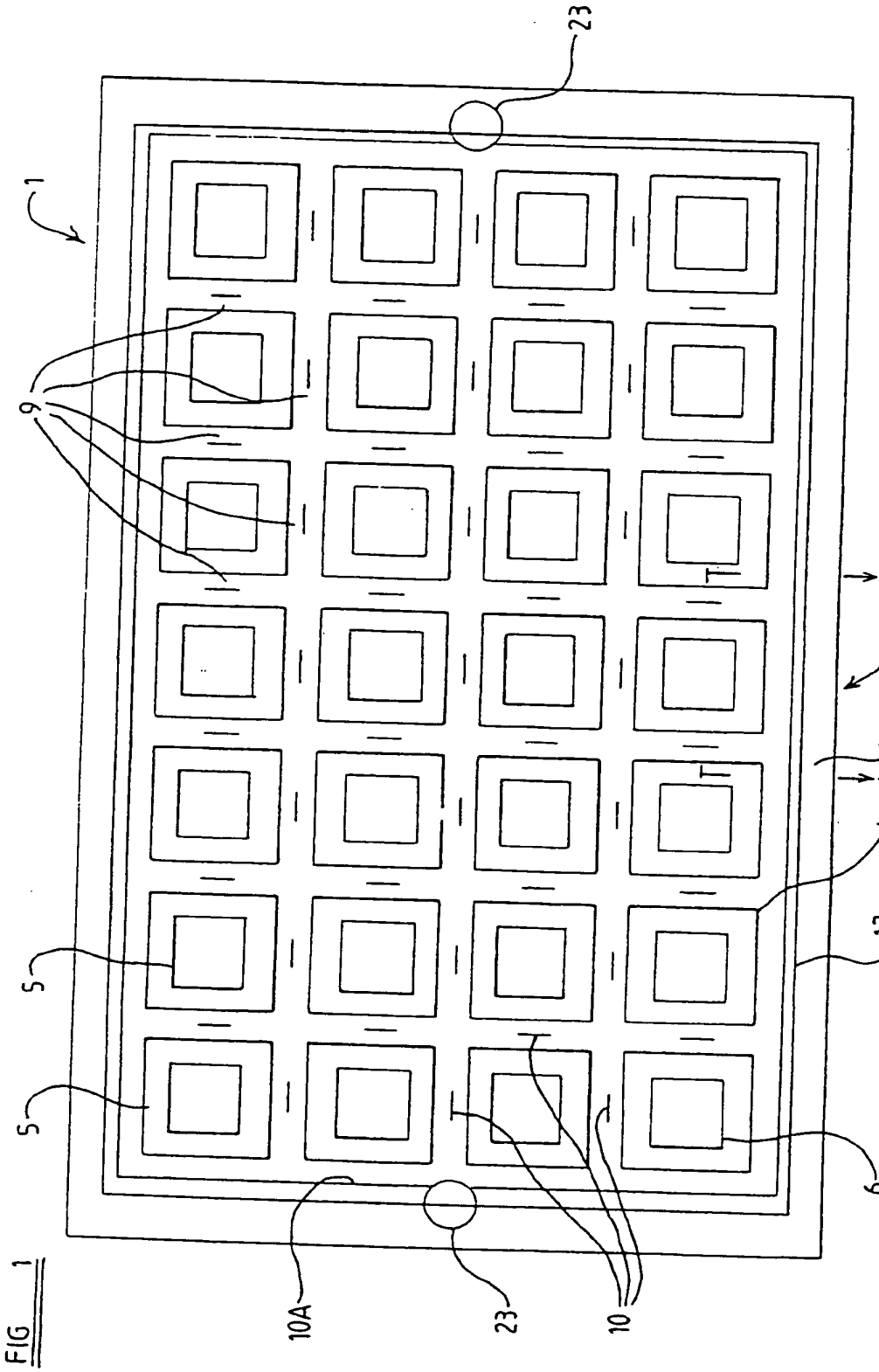

FIG 1

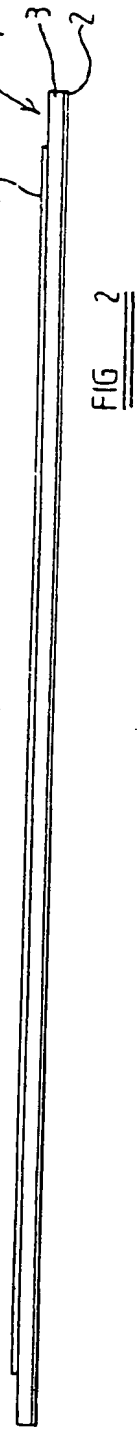

FIG 2

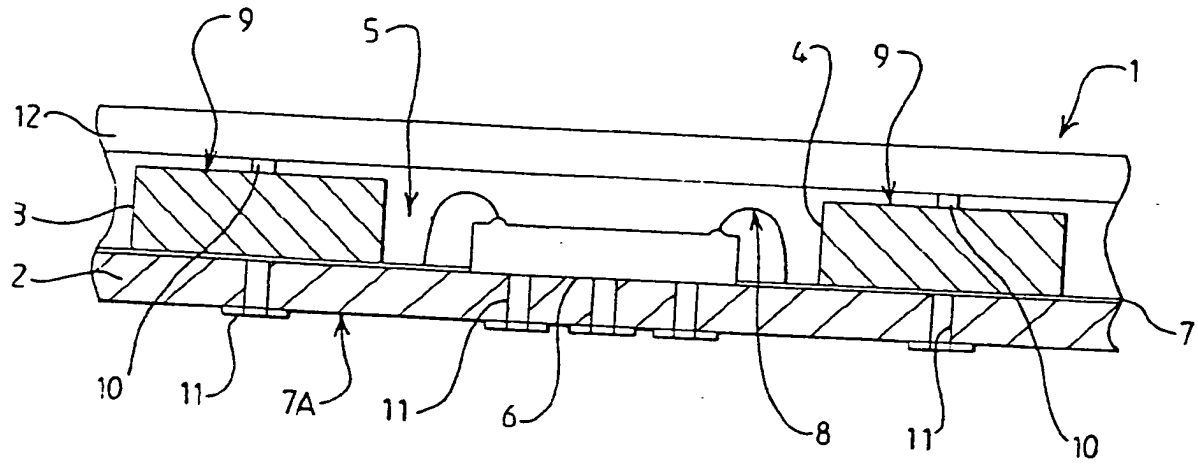

FIG 3

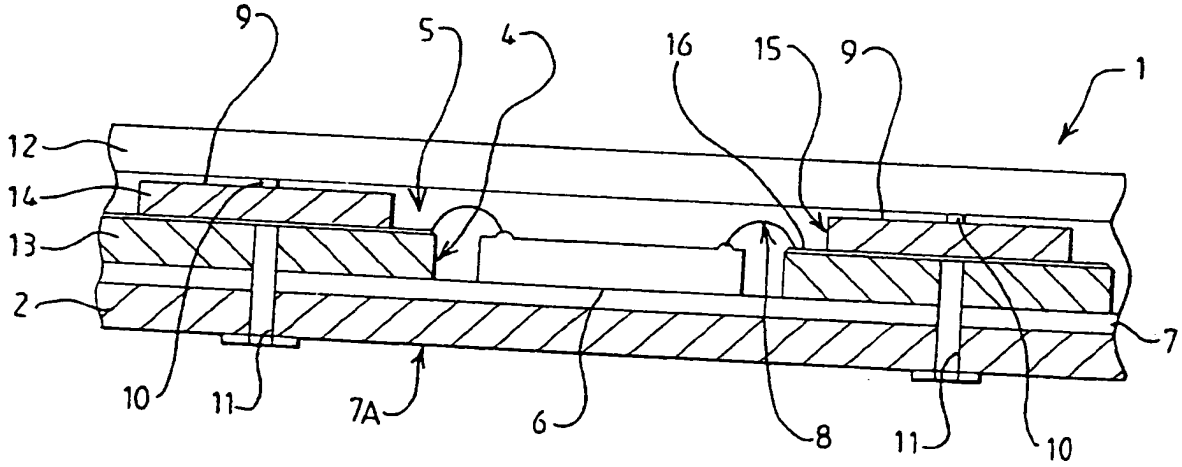

FIG 4

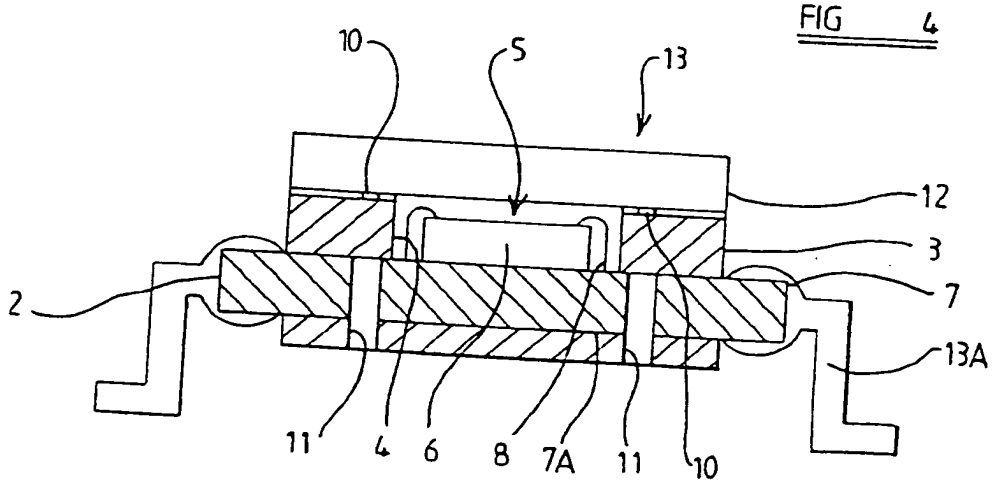

FIG 5

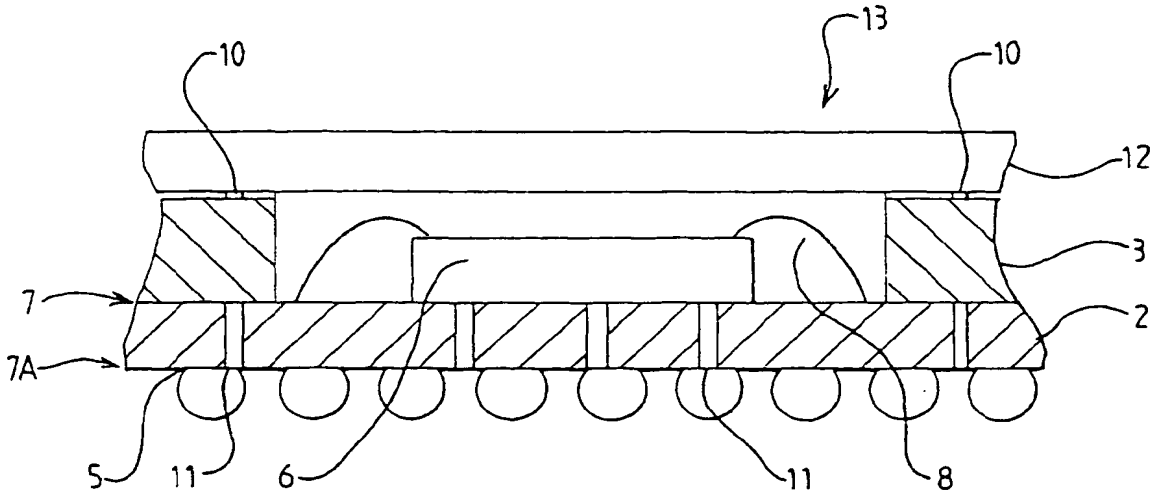

FIG 6

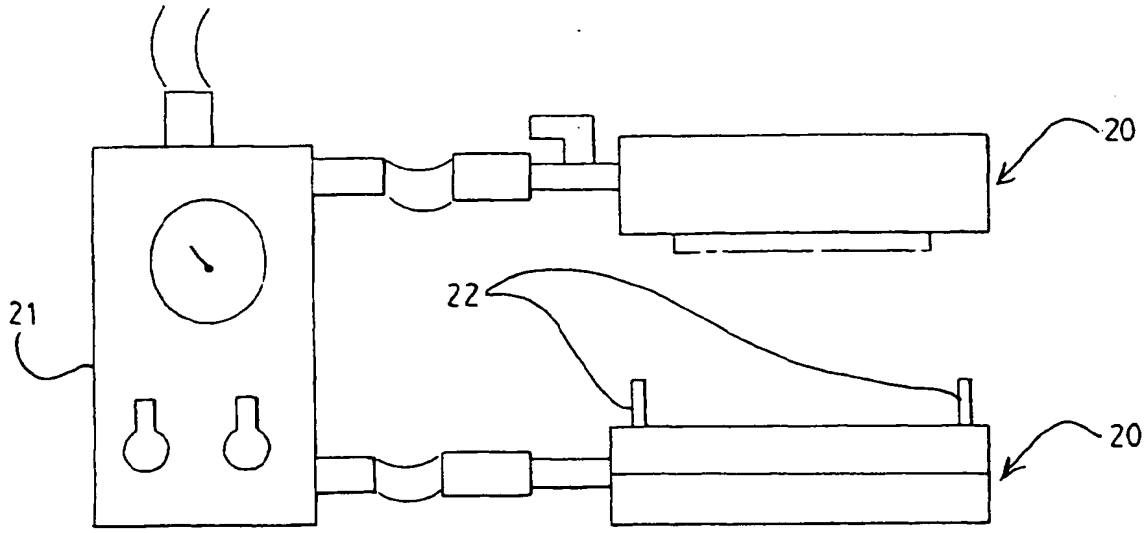

FIG 7

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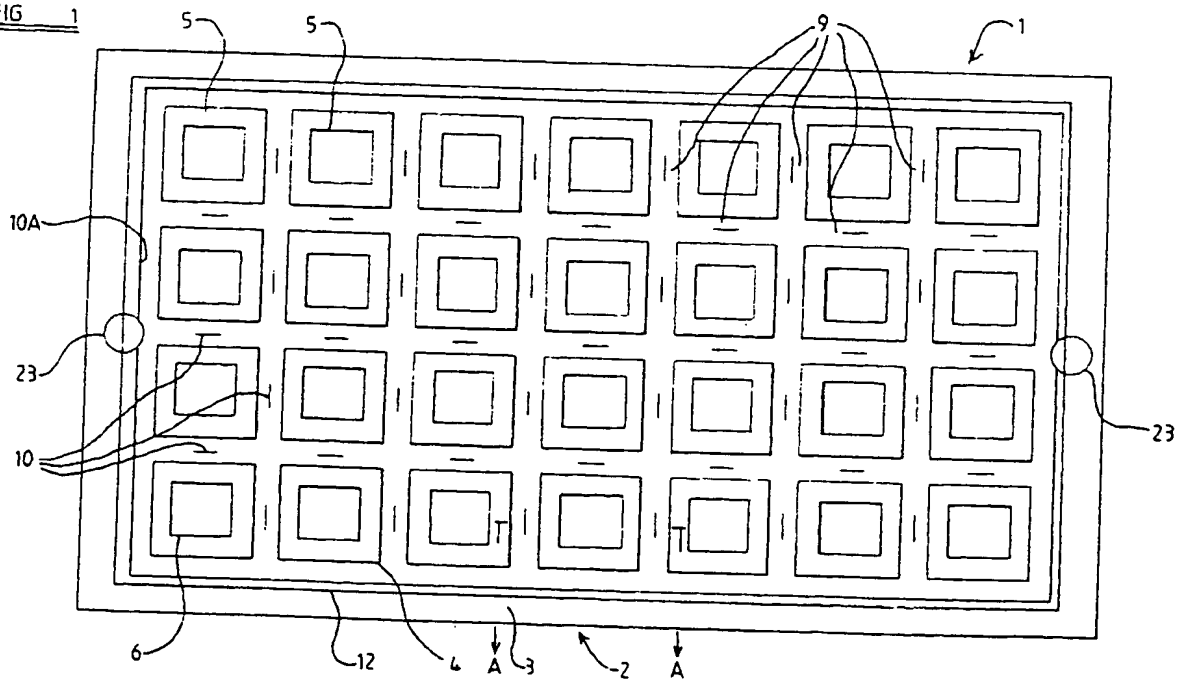
FIG 1



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EUROPEAN SEARCH REPORT

Application Number
EP 99 30 6807

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 386 (E-812), 25 August 1989 (1989-08-25) -& JP 01 134956 A (HITACHI LTD), 26 May 1989 (1989-05-26)	1-4,7, 15,17, 18,21-24	H01L23/10 H01L33/00 H01L31/0203
Y	* abstract *	12,13	
X	DE 196 22 650 A (CIRCUIT COMPONENTS INC) 12 December 1996 (1996-12-12)	1,5-7, 15,18,	
A	* column 4, line 22 - line 68; figures 1,6 *	19,21 1,21	
Y	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 11, 28 November 1997 (1997-11-28) -& JP 09 199623 A (NGK SPARK PLUG CO LTD), 31 July 1997 (1997-07-31) * the whole document *	12	
X	EP 0 609 062 A (TRW INC) 3 August 1994 (1994-08-03)	1-4,7, 15,17,	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
	* page 4, column 5, line 51 - column 6, line 52; figures 1,4-6 *	18,21-24	H01L
Y	LYMAN J: "RESIN DAM PROTECTS CHIPS IN MOLDED PGA" , ELECTRONIC DESIGN, PENTON PUBLISHING, CLEVELAND, OH, US, VOL. 37, NR. 2, PAGE(S) 29 XP000028938 ISSN: 0013-4872 * the whole document *	13	

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 March 2002	ZEISLER, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

1-7,12-19,21-24

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 99 30 6807

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-7,12-19,21-24

   An electronic component package assembly

2. Claims: 8-11,20

   A optical component package assembly comprising a transparent lid or base having a cut-out covered with transparent material

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 99 30 6807

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

04-03-2002

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